# CMS Pixel ROC PSI46 V2 Summary Of Tests Description, Selection Criteria

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## Introduction

This document is a summary list of on wafer test performed on PSI46V2 chip and selection criteria used. For in-depth details please check any of the following documents in FPIX data base: 776, 606, 542, 444, 443, 442, 429, 428, 329, 331, 326, 325, 324, 323, 322 and 233.

## 1. Testing program review

The same hardware and software instruments as in previous test reports will be used for future wafer test. The overall testing program flow is presented below.

1. Interface board setup – I2C address, frequency, CAL, TRIG, TOKEN delays. Power on PSI46V2 chip and issue ROC RESET pulse.
2. Measure misc. supply currents and voltages 'before setup'.
3. Download chip configuration – program all DAC registers with default values and set all pixel enable bits and set all pixel trim bits to 0x08.
4. Measure misc. supply currents and voltages 'after setup'.
5. Do token out test.
6. Do I2C test.
7. Do I-V curve test for Vana DAC register to set Iana=24mA+-1mA.
8. Do DAC registers' linearity test.
9. Do Vcaldel and Vthcomp scan to find optimal values.
10. Do Vcal and MaskTrim loop test for each of the 4160 pixels.
11. Do data buffer test for each double column.
12. Do time stamp buffer test for each double column.
13. Do WBC test.

All tests are executed in this order, regardless of the results of previous tests, with the following exceptions:

1. In step 4, if the digital or the analog current supply are <5mA or >55mA the chip testing is aborted.
2. In step 5 if token out test fails the chip testing is aborted.

A FailCode integer number (18bits in binary) is associated with each chip for qualification. FailCode's bits are set if one of the above tests fails, as follows:

Bit 0 is set when digital supply current is too low.
Bit 1 is set when digital supply current is too high.
Bit 2 is set when analog supply current is too low.
Bit 3 is set when digital supply current is too high.
Bit 4 is set when DAC Linearity Test negative deviation is too low.
Bit 5 is set when DAC Linearity Test positive deviation is too high.
Bit 6 is set when DAC Linearity Test found a response length error.
Bit 7 is set when DAC Linearity Test found a FIFO full flag error.
Bit 8 is set when Token Out Test failed.
Bit 9 is set when I2C Test failed.
Bit 10 is set when I-V Curve failed.
Bit 11 is set when Time Stamp Buffer Test failed.
Bit 12 is set when Data Buffer Test failed.
Bit 13 is set when WBC Register Test failed.
Bit 14 is set when 1-5 pixels failed.
Bit 15 is set when 6-10 pixels failed.
Bit 16 is set when 11-20 pixels failed.
Bit 17 is set when >20 pixels failed.

The wafer testing program is reading analog cut values from a separate file. Currently we have implemented the following analog cuts:

1. Digital supply current 'after setup' must be within 5mA to 55mA.
2. Analog supply current 'after setup' must be within 5mA to 55mA.
3. DAC linearity deviation must be within +-1%.
4. Read out charge must be higher than 2200 ADC counts.

While the chips are tested, a couple of files are generated as follows:

1. Special .xml files with miscellaneous measurement values for data base storage (see doc 542).
2. One detailed report file per chip. This is a file resident on probe station's computer and it contains more information than is currently passed to data base.
3. One hex file per chip with raw binary data from tester hardware. This file can be loaded off line by the testing software if we want to apply different data analysis and or selection algorithms.
4. One special file intended for automatic ink dot placement. Currently the wafers are inked off line, after analyzing data and sorting tested chips in classes.
5. One report file for all chips tested on one wafer.

The last two files can be used offline by other software to analyze data, select chips in classes and provide appropriate information for bump bonding company.

## 2. Test steps and associated selection criteria

For more technical details related to each test see doc 329.

2.1. Interface board setup. Not applicable.

2.2. Measure misc. supply currents and voltages 'before setup'. Not applicable.

2.3. Download chip configuration. Not applicable.

But please note that we configure all pixels to be 'alive' (unmasked) while PSI approach is to configure all pixels to be 'killed' (masked).

2.4. Measure misc. supply currents and voltages 'after setup'.

Analog and digital currents are required to be within 5mA and 55mA. If outside these limits, the test is aborted and the chip is considered failed.

Bit 0 is set when digital supply current is too low.
Bit 1 is set when digital supply current is too high.
Bit 2 is set when analog supply current is too low.
Bit 3 is set when digital supply current is too high.

2.5. Token Out test.

This test checks the ROC response to a Token In. If no Ultra Black, Black and Last DAC are detected, the test is aborted and the chip is considered failed.

Bit 8 is set when Token Out Test failed.

2.6. I2C test.

This test checks the functionality of all 16 I2C addresses. If one or more of the I2C address is found not functional, the test is considered failed but the chip testing is continued.

Bit 9 is set when I2C Test failed.

2.7. I-V curve test for Vana DAC register.

This test seeks for a Vana register setting for which the analog power supply current of ROC is within 23mA and 25mA. All further tests are performed using this Vana setting. If Iana can't be squeezed inside the 23 to 25mA range, the test is considered failed but the chip testing is continued.

Bit 10 is set when I-V curve test failed.

2.8. DAC registers' linearity test.

The purpose of this test is to check the functionality of each DAC. To do that, the test writes five values to each DAC register and check the last DAC response. For an eight bit DAC the values written are hex 00, 40, 80, C0 and FF. For a four bit DAC the values written are hex 0, 4, 8, C and F. The last DAC responses are interpolated with a linear function. If the maximum deviation between the measured value and the linear fit is larger than +-1% the test is considered failed but the chip testing is continued.

Bit 4 is set when DAC Linearity Test negative deviation is too low.
Bit 5 is set when DAC Linearity Test positive deviation is too high.
Bit 6 is set when DAC Linearity Test found a response length error.
Bit 7 is set when DAC Linearity Test found a FIFO full flag error.

The following registers are excluded from this test, since usually the chip is losing functionality while the registers are scanned: voltage regulator registers Vdig and Vana, pixel readout register Vbiasbus and chip control register Ctrl.

There are three registers with a systematic higher nonlinearity: chip readout pulse height VIbias_PH, chip readout single ended output level VIbias_roc and temperature control register.

This test is not implemented by PSI.

## 2.9. Do Vcaldel and Vthcomp scan to find optimal values.

This is a new test we introduced with the aim to find, for each chip, the optimal settings of Vcaldel and Vthcomp registers. To find these settings, one pixel in the center of the pixel's array (column 26, row 40) is monitored when both registers are scanned between 0x20 and 0xA0 in steps of 0x08 as in the following test report example. The Vcal setting is fixed to 0x80.

```
|**********************************************************************
OptimizeVthcompVcaldel Test Report
Vcaldel(Xaxis)=0x            20             a0             08
Vthcomp(Yaxis)=0x            20             a0             08
|-----------------|
|-----------------|
|-----X-----------|
|-----X-----------|
|----XXXX---------|
|-----XXXXX-------|
|-----XXXXXXXXX---|
|-----XXXXXXXXX---|
|-----XXXXXXXXX---|
|------XXXXXXXX---|
|-------XXXXXXX---|
|--------XXXXXX---|
|----------XXXX---|
|-------------X---|
|-----------------|
|-----------------|
|-----------------|
Vcaldel-optimal=0x68 decimal  104
Vthcomp-optimal=0x5F decimal  95
|**********************************************************************
```

Using the center of mass formulas, the optimum values are calculated. The two DACs are programmed with these values for all following tests.

## 2.10. Vcal and MaskTrim loop test for each of the 4160 pixels.

The purpose of this test is to check the functionality of each pixel. It is shortly described here just for the record. For more details please refer to previous reports. Each of the 4160 pixels' responses is measured in a double loop scan of Vcal and MaskTrim registers as follows:

1. Set the pixel mask bit '1' (pixel enabled) and pixel trim bits to a default value masktrimmin. Set the Vcal DAC register to a default value vcalmin. Set this pixel to calibrate via calibrate capacitor injection charge.

2. Start to increase Vcal in steps of vcalstep. Do chip readout at each step and check the result. If pixel responds with a hit, continue to step 3. If not loop on step 2 until the Vcal reaches the default vcalmax value and then continue to step 3.
3. Set Vcal to vcalmax and disable the pixel. Do chip readout and check the result.
4. Re-enable the pixel, set the Vcal to vcalmin, increment the trim bits with masktrimstep and jump back to step 2.
5. When trim bits reach masktrimmax this pixel exercise is complete. Execute clear calibration command and repeat the full test for a new pixel cell. Do this for all 4160 pixels.

This test is somehow different from the approach used at PSI. They do a similar but not identical trim sweep. Also, the other register involved in their test is not Vcal but Vthcomp.

A report example for this test looks like in following pictures.

The L1, L2, L3, L4, L5 and L6 represent the six analog levels used to encode the pixel's row and column address. The charge readout is Q. Both are represented in counts, after ADC conversion by the tester board. All measured pixels are included in this statistics. Then, after the pixel is qualified as good or defective, the same six analog levels are reported only on good pixels and separately for row and column addresses. Also the charge (Q), black, ultra black and pedestal levels (BK, UBK, PED) are reported as well as the interpolation line's slope, intercept and correlation (TVS, TVI, TVR2) for the Vcal vs. trim bits dependence. All the defective pixels are then listed, starting with first column and following a defect type encoding explained in previous reports. Finally, the total number of failed pixels is reported together with a pixel map of the chip.

Bit 14 is set when 1-5 pixels failed.
Bit 15 is set when 6-10 pixels failed.
Bit 16 is set when 11-20 pixels failed.
Bit 17 is set when >20 pixels failed.

```
Pixel Test Report
Pixel Test Setup Parameters
masktrimmin =0x84
masktrimmax =0x90
masktrimstep=0x04
vcalmin     =0x40
vcalmax     =0xc0
vcalstep    =0x10
```

REPORTING ANALOG LEVELS HISTOGRAM
column/row address = 6 clusters, charge = 1 cluster

| | BIN(min) | BIN(max) | ADDRESS | CHARGE | VCAL | BASELINE | ULTRABLACK | BLACK |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 15 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2 | 16 | 31 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3 | 32 | 47 | 0 | 0 | 0 | 0 | 0 | 0 |
| 4 | 48 | 63 | 0 | 0 | 0 | 0 | 0 | 0 |
| 5 | 64 | 79 | 0 | 0 | 0 | 0 | 0 | 0 |
| 6 | 80 | 95 | 0 | 0 | 0 | 0 | 0 | 0 |
| 7 | 96 | 111 | 0 | 0 | 0 | 0 | 0 | 0 |
| 8 | 112 | 127 | 0 | 0 | 0 | 0 | 0 | 0 |
| 9 | 128 | 143 | 0 | 0 | 0 | 0 | 0 | 0 |
| 10 | 144 | 159 | 0 | 0 | 281 | 0 | 0 | 0 |
| 11 | 160 | 175 | 0 | 0 | 4080 | 0 | 0 | 0 |
| 12 | 176 | 191 | 0 | 0 | 5378 | 0 | 0 | 0 |
| 13 | 192 | 207 | 0 | 0 | 2461 | 0 | 0 | 0 |
| 14 | 208 | 223 | 0 | 0 | 257 | 0 | 0 | 0 |
| 15 | 224 | 239 | 0 | 0 | 0 | 0 | 0 | 0 |
| 16 | 240 | 255 | 0 | 0 | 0 | 0 | 0 | 0 |
| 17 | 256 | 271 | 0 | 0 | 0 | 0 | 0 | 0 |
| ..... | | | | | | | | |
| 117 | 1856 | 1871 | 0 | 0 | 0 | 0 | 0 | 0 |
| 118 | 1872 | 1887 | 0 | 0 | 0 | 0 | 0 | 0 |
| 119 | 1888 | 1903 | 5358 | 0 | 0 | 0 | 0 | 0 |
| 120 | 1904 | 1919 | 6719 | 0 | 0 | 0 | 0 | 0 |
| 121 | 1920 | 1935 | 0 | 0 | 0 | 0 | 0 | 0 |
| 122 | 1936 | 1951 | 0 | 0 | 0 | 0 | 0 | 0 |
| 123 | 1952 | 1967 | 0 | 0 | 0 | 0 | 0 | 0 |
| 124 | 1968 | 1983 | 0 | 0 | 0 | 0 | 0 | 0 |
| 125 | 1984 | 1999 | 0 | 0 | 0 | 0 | 0 | 0 |
| 126 | 2000 | 2015 | 0 | 0 | 0 | 0 | 0 | 0 |
| 127 | 2016 | 2031 | 0 | 0 | 0 | 0 | 0 | 0 |
| 128 | 2032 | 2047 | 0 | 0 | 0 | 0 | 0 | 0 |
| 129 | 2048 | 2063 | 0 | 0 | 0 | 0 | 0 | 0 |
| 130 | 2064 | 2079 | 344 | 0 | 0 | 829 | 0 | 12456 |
| 131 | 2080 | 2095 | 12876 | 0 | 0 | 11628 | 0 | 1 |
| 132 | 2096 | 2111 | 22 | 0 | 0 | 0 | 0 | 0 |
| 133 | 2112 | 2127 | 0 | 0 | 0 | 0 | 0 | 0 |
| 134 | 2128 | 2143 | 0 | 0 | 0 | 0 | 0 | 0 |
| 135 | 2144 | 2159 | 0 | 0 | 0 | 0 | 0 | 0 |
| 136 | 2160 | 2175 | 0 | 0 | 0 | 0 | 0 | 0 |
| 137 | 2176 | 2191 | 0 | 0 | 0 | 0 | 0 | 0 |
| 138 | 2192 | 2207 | 0 | 0 | 0 | 0 | 0 | 0 |
| 139 | 2208 | 2223 | 0 | 0 | 0 | 0 | 0 | 0 |
| 140 | 2224 | 2239 | 0 | 0 | 0 | 0 | 0 | 0 |
| 141 | 2240 | 2255 | 4 | 0 | 0 | 0 | 0 | 0 |
| 142 | 2256 | 2271 | 11678 | 0 | 0 | 0 | 0 | 0 |
| 143 | 2272 | 2287 | 356 | 0 | 0 | 0 | 0 | 0 |
| 144 | 2288 | 2303 | 0 | 0 | 0 | 0 | 0 | 0 |
| 145 | 2304 | 2319 | 0 | 0 | 0 | 0 | 0 | 0 |
| 146 | 2320 | 2335 | 0 | 0 | 0 | 0 | 0 | 0 |
| 147 | 2336 | 2351 | 0 | 0 | 0 | 0 | 0 | 0 |
| 148 | 2352 | 2367 | 0 | 0 | 0 | 0 | 0 | 0 |
| 149 | 2368 | 2383 | 0 | 0 | 0 | 0 | 0 | 0 |
| 150 | 2384 | 2399 | 0 | 0 | 0 | 0 | 0 | 0 |
| 151 | 2400 | 2415 | 0 | 0 | 0 | 0 | 0 | 0 |
| 152 | 2416 | 2431 | 0 | 1 | 0 | 0 | 0 | 0 |
| 153 | 2432 | 2447 | 10485 | 2 | 0 | 0 | 0 | 0 |
| 154 | 2448 | 2463 | 1090 | 22 | 0 | 0 | 0 | 0 |
| 155 | 2464 | 2479 | 0 | 87 | 0 | 0 | 0 | 0 |
| 156 | 2480 | 2495 | 0 | 233 | 0 | 0 | 0 | 0 |
| 157 | 2496 | 2511 | 0 | 657 | 0 | 0 | 0 | 0 |
| 158 | 2512 | 2527 | 0 | 1415 | 0 | 0 | 0 | 0 |
| 159 | 2528 | 2543 | 0 | 2487 | 0 | 0 | 0 | 0 |
| 160 | 2544 | 2559 | 0 | 2935 | 0 | 0 | 0 | 0 |
| 161 | 2560 | 2575 | 0 | 2390 | 0 | 0 | 0 | 0 |
| 162 | 2576 | 2591 | 0 | 1399 | 0 | 0 | 0 | 0 |
| 163 | 2592 | 2607 | 0 | 688 | 0 | 0 | 0 | 0 |
| 164 | 2608 | 2623 | 6856 | 242 | 0 | 0 | 0 | 0 |
| 165 | 2624 | 2639 | 1400 | 53 | 0 | 0 | 0 | 0 |
| 166 | 2640 | 2655 | 0 | 5 | 0 | 0 | 0 | 0 |
| 167 | 2656 | 2671 | 0 | 1 | 0 | 0 | 0 | 0 |
| 168 | 2672 | 2687 | 0 | 0 | 0 | 0 | 0 | 0 |
| 169 | 2688 | 2703 | 0 | 0 | 0 | 0 | 0 | 0 |
| 170 | 2704 | 2719 | 0 | 0 | 0 | 0 | 0 | 0 |
| 171 | 2720 | 2735 | 0 | 0 | 0 | 0 | 0 | 0 |
| 172 | 2736 | 2751 | 0 | 0 | 0 | 0 | 0 | 0 |
| 173 | 2752 | 2767 | 0 | 0 | 0 | 0 | 0 | 0 |
| 174 | 2768 | 2783 | 745 | 0 | 0 | 0 | 0 | 0 |
| 175 | 2784 | 2799 | 5152 | 0 | 0 | 0 | 0 | 0 |
| 176 | 2800 | 2815 | 0 | 0 | 0 | 0 | 0 | 0 |
| 177 | 2816 | 2831 | 0 | 0 | 0 | 0 | 0 | 0 |

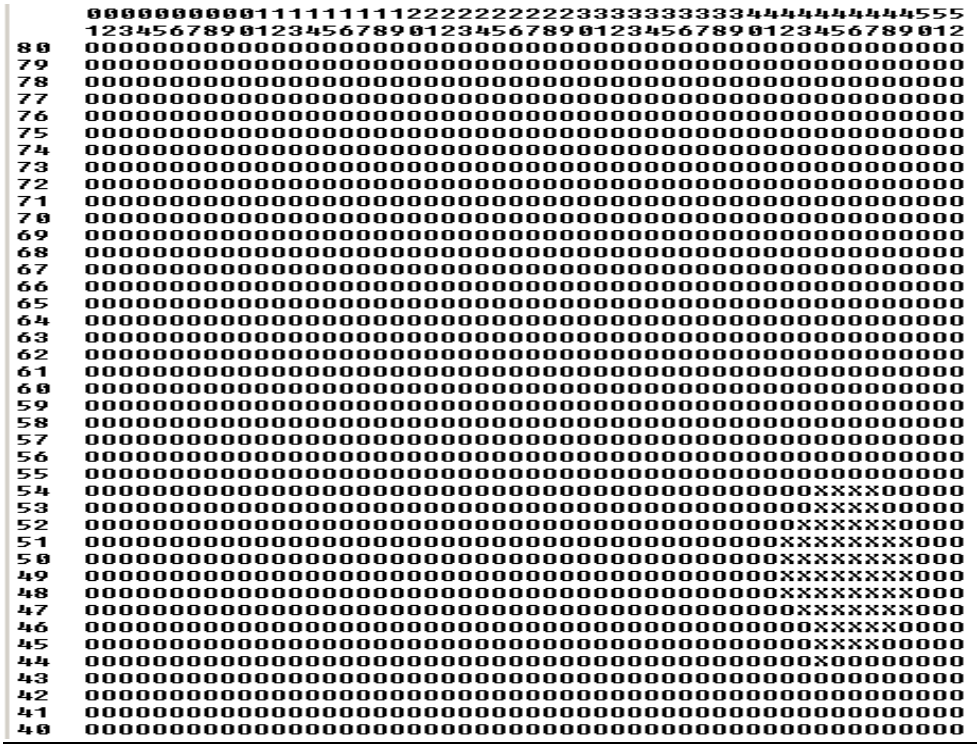
| | LEV(min) | LEV(max) | RANGE | GAP |
|---|---|---|---|---|
| L1 | 1887 | 1920 | 33 | |
| L2 | 2063 | 2112 | 49 | 143 |
| L3 | 2239 | 2288 | 49 | 127 |
| L4 | 2431 | 2464 | 33 | 143 |
| L5 | 2607 | 2640 | 33 | 143 |
| L6 | 2767 | 2800 | 33 | 127 |
| Q | 2415 | 2672 | 257 | |

| PARAM | AVERAGE | MIN | MAX | ENTRIES |
|---|---|---|---|---|
| TVS | 2.97 | 2 | 4 | 4138 |
| TVI | 150.05 | 128 | 186.67 | 4138 |
| TVR2 | 0.93 | 0.87 | 1 | 4138 |
| PED | 2081 | 2079 | 2083 | 4138 |
| UBK | 1388 | 1385 | 1392 | 4138 |
| BK | 2075 | 2071 | 2078 | 4138 |
| Q | 2551 | 2457 | 2645 | 4138 |
| VCAL | 174 | 155 | 203 | 4138 |
| CLev1 | 1902 | 1897 | 1910 | 1740 |
| RLev1 | 1906 | 1897 | 1916 | 2245 |
| CLev2 | 2083 | 2078 | 2090 | 1748 |
| RLev2 | 2086 | 2077 | 2096 | 2390 |
| CLev3 | 2262 | 2256 | 2267 | 1596 |
| RLev3 | 2265 | 2256 | 2275 | 2407 |
| CLev4 | 2441 | 2436 | 2446 | 1598 |
| RLev4 | 2444 | 2435 | 2453 | 2253 |
| CLev5 | 2618 | 2612 | 2623 | 955 |
| RLev5 | 2621 | 2613 | 2630 | 1793 |
| CLev6 | 2785 | 2781 | 2789 | 639 |
| RLev6 | 2788 | 2779 | 2796 | 1326 |

REPORTING DEFECTIVE PIXELS ON EACH COLUMN

COL1 found 4 defective pixels:ROW75N3,ROW77N3,ROW78N3,ROW80N2,N3,
COL2 found 1 defective pixels:ROW80N3,
COL3 found 2 defective pixels:ROW79N3,ROW80N3,
COL4 found 1 defective pixels:ROW80N3,
COL5 found 1 defective pixels:ROW80N3,
COL6 found 1 defective pixels:ROW80N3,
COL7 found 1 defective pixels:ROW80N3,
COL9 found 1 defective pixels:ROW80N3,
COL12 found 1 defective pixels:ROW80N3,
COL13 found 1 defective pixels:ROW80N3,
COL15 found 1 defective pixels:ROW80N3,
COL16 found 1 defective pixels:ROW80N3,
COL18 found 1 defective pixels:ROW80N3,
COL21 found 1 defective pixels:ROW80N3,
COL22 found 1 defective pixels:ROW80N3,
COL25 found 1 defective pixels:ROW80N3,
COL46 found 1 defective pixels:ROW80N3,
COL52 found 1 defective pixels:ROW80N3,

TOTAL NUMBER OF DEFECTIVE PIXELS = 22 from 4160




Partial pixel map of chip 43_3 on wafer#5

The bottom line is that, after this test, each pixel is assigned an encoded error string. If the pixel is good, the error string attached is null. The conditions that make a pixel error code not null are listed below, with their alpha numeric encoding scheme where 'n' is an integer representing the masktrim setting loop number at which the condition failed.

Fn or FDn => Hardware error.

Cn => Column not found (data is missing).

Nn => Pixel is not responding to any Vcal (within vcalmin and vcalmax).

Mn0m => Pixel is responding with m hits, not only one hit. PSI calls this a noisy pixel.

Dn0m => Pixel responding when it is disabled ('masked' or 'killed').

LnC0, LnC1, LnA0, LnA1, LnA2 => Pixel has incorrect Column or Row address level.

Qn => Pixel charge is less than a predefined value.

## 2.11. Data buffer test.

This test checks the functionality of each double column's data buffer. The data buffer must be capable of retaining a maximum of 31 triggers, then it must reset on 32$^{nd}$ trigger.

Bit 12 is set when Data Buffer Test failed.

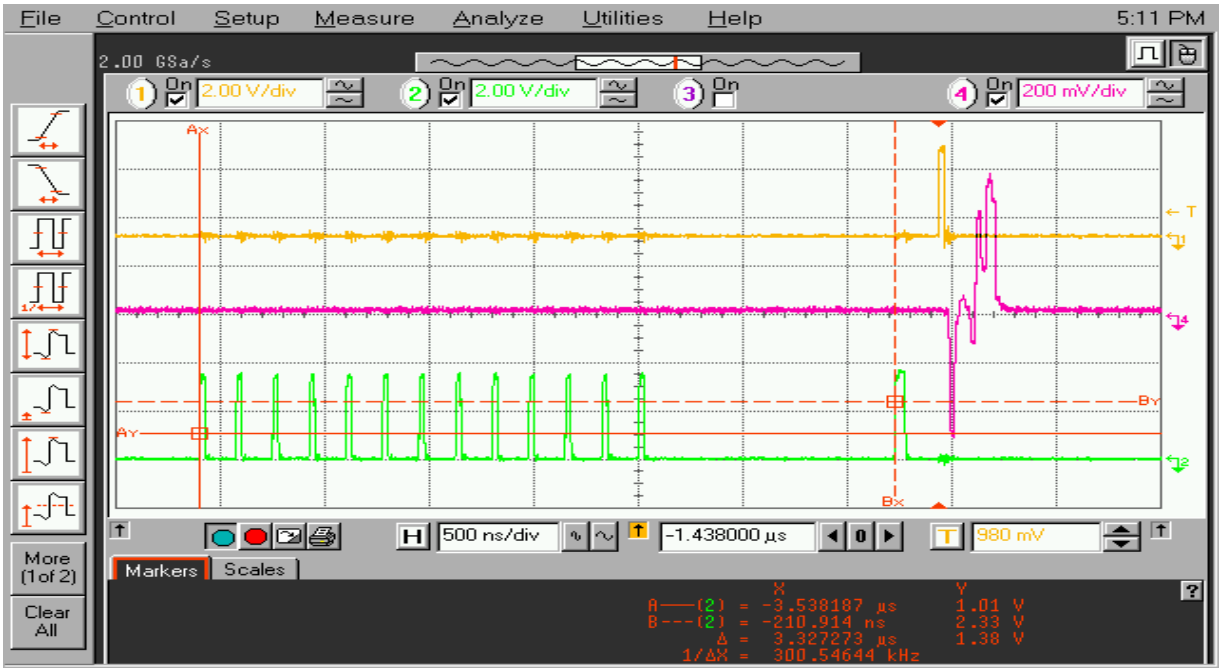
## 2.12. Time stamp buffer test.

This test checks the functionality of each double column's time stamp buffer. The implementation of this test follows PSI suggestions but it is, in our opinion, more comprehensive than their test procedure. The test is repeated for each double column. In a first step one good

pixels is searched for a given double column. Then a burst of 15 CAL pulses followed by a TRIG is sent to the chip and then the chip is readout and the response data length is checked. This sequence is repeated by moving the TRIG pulse such as to point to the first CAL of the burst, then to the second and so on. We must see in the readout just one hit in all these cases. When TRIG is pointing to the 13$^{th}$ CAL, where the time stamp buffer was reset, we must read out no hits at all. See also the following oscilloscope picture for TOKENIN, CONTROL and ANALOG_OUT signals. The distance between two CAL pulses in the burst is 7*CLK period.

It is worth to be outlined that, because of the calibration pulse circuitry limitations inside the chip, this test does not work properly at clock frequencies higher than 5MHz. This was confirmed by chip designers at PSI. All tests we are performing are done at 40MHz clock frequency, the only exception is this time stamp buffer test.

Bit 11 is set when Time Stamp Buffer Test failed.




2.13. WBC register test.

The implementation of this test follows PSI test procedure. This test is NOT repeated for each double column since the WBC register is only one general register in chip's architecture. In a first step one good pixels is searched anywhere inside the pixel array, starting with the first chip column and row. On that good pixel the test is repeated for the following 8 values of WBC: 0x08, 0x09, 0x0A, 0x0C 0x10, 0x20, 0x40, 0x80. For each of these WBC settings, the CAL pulse position is fixed and the TRIG position is loop through all values between 0x08 and 0xF8. When the distance between CAL and TRIG matches the WBC number, a hit must be readout. No hit should be present in all the other cases.

Bit 13 is set when WBC Register Test failed.

## Conclusion

A summary list of on wafer tests performed on PSI46V2 chip and selection criteria was presented. With the exception of Vcaldel and Vthcomp optimization presented in paragraph 2.9 and the pixel charge test presented in paragraph 2.10 all the other tests and criteria presented were applied on wafers tested so far.

For in-depth details please check the documents listed in the Introduction section. In particular doc#606 presents the test results for all ROC wafers tested so far (wafers 3 to 9). For each wafer two files are reported in this document:

1. The first file is a *.jpg wafer map presenting chip location on wafer and their assignment to different pass/fail classes.
2. The second file is a text file listing the chips grouped in classes based on their analog levels.

These two files are currently used as guidelines for the bump bonding company.